DETAILED ACTION

1. This office action is in response to the claim amendment and remarks filed on June 08, 2009. Claims 1, 9, 17 and 21 are currently amended; and none of the claims are currently cancelled or newly added. Therefore, claims 1 and 3-23 are currently pending in this application.

2. All previously outstanding objections and/or rejections to the Applicant's disclosure and/or claims not contained in this office action have been respectfully withdrawn by the Examiner hereto.

3. Applicant's arguments with respect to amended claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 and 3-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 3-23 contain the trademark or trade name XScale. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe processor/core architecture and, accordingly, the identification/description is indefinite. For purpose examination, Examiner interpreting the term "Xscale core architecture" as any type of architecture.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 8-12, 17-19 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mallick (USPN: 5,953,520) in view of Okada (USPN: 6,275,917).

As per claim 1, Mallick teaches a method, comprising: receiving a virtual page number lookup request at a virtual Translation Lookaside Buffer (TLB) (i.e. receiving logical (effective) address at the MMUs 56 and 58 in Fig. 2), wherein the virtual TLB (i.e. the combination of ITLB and DTLB, 59 and 57 in Fig. 2) includes an instruction TLB (59 in Fig. 2) and a data TLB (57 in Fig. 2), wherein the TLB is configured to operate in a processor having an Xscale core architecture (i.e. CPU 4 in Fig. 1; CPU/processor having Intel x86 architecture; see Col. 13, lines 13+); performing a lookup of the virtual page number in the virtual TLB; and returning a physical page number corresponding to the virtual page number in the virtual TLB (i.e. if miss occurs, then an exception is taken and the page table is searched for the matching PTE; see Col. 12, line 21 - Col. 13, line 7 and Fig. 2).

However, Mallick does not teach that the lookup of the virtual page number in the instruction TLB and the data TLB is performed simultaneously. Okada, on the other hand, discloses about performing the address translation (i.e. searching in TLB) in both ITLB and DTLB in parallel (see Col. 4, lines 50-55 and Col. 8, lines 21-24). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to implement the teaching of Okada in the method taught by Mallick so the lookup is performed in parallel instead of one-by-one so the overall translation process is expedited, especially when there is no match found in the first TLB.

As per claims 9-11, 17 and 21, refer rejection of claim 1. Claims 9-11, 17 and 21 are also rejected based on the same rationale as the rejection of claim 1.

As per claims 3, 12, 18-19 and 22, the combination of Mallick and Okada teaches the claimed invention as described above and furthermore, Mallick teaches about performing a page table lookup if the virtual address is not found in the virtual TLB (i.e. if miss occurs, then an exception is taken and the page table is searched for the matching PTE; see Col. 13, lines 2-7).

As per claim 8, the combination of Mallick and Okada teaches the claimed invention as described above and furthermore, Mallick teaches that the virtual page number lookup request is received from one of a Data Memory Management Unit (DMMU) or an Instruction Memory Management Unit (IMMU) (see Col. 12, lines 37-40).

7. Claims 4-7, 13-16, 20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mallick in view of Okada, further in view of Augsburg et al. (USPN: 2007/0094476) hereinafter, Augsburg.

As per claims 4 and 5, the combination of Mallick and Okada teaches the claimed invention as described above. However, both Mallick and Okada failed to disclose about updating the virtual TLB with the virtual page number and a corresponding physical page number resulting from the page table lookup, wherein updating the virtual TLB includes: updating the data TLB if a physical address corresponding to the virtual address has stored data; and updating the instruction TLB if the physical address corresponding to the virtual address has stored an instruction.

Augsburg, on the other hand, teaches about having multiple TLBs and also separate ITLB and DTLB; and when the desired virtual address generates TLB miss, both upper and lower TLBs are updated with the new address information retrieved from the page table (see paragraph [0004] and the abstract). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to implement the teachings of Augsburg in the method taught by the combination of Mallick and Okada so the future virtual TLB miss for the same virtual address is avoided.

As per claims 13-14, 20 and 23, refer rejection of claims 4 and 5. Claims 13-14, 20 and 23 are also rejected based on the same rationale as the rejection of claims 4 and 5.

As per claims 6 and 15, the combination of Mallick, Okada and Augsburg teaches the claimed invention as described above, but failed to specifically disclose about using a round robin algorithm to update the virtual TLB. Updating TLB using different algorithms such as LRU, MRU, FIFO, round-robin etc. Further, neither Applicant nor the specification disclose that using a round robin algorithm to update the virtual TLB as claimed here is critical, i.e. neither Applicant nor the specification disclose that by updating the virtual TLB differently would downgrade the functionality or performance of the cache memory of the claimed method and apparatus. Therefore, updating the virtual TLB as claimed is considered to be an obvious matter of design choice.

As per claims 7 and 16, the combination of Mallick, Okada and Augsburg teaches the claimed invention as described above and furthermore, Augsburg teaches that the page table lookup is performed by an operating system (see paragraphs [0002] and [0023]).

Remarks

8. As to the remark, Applicant asserted that

(a) Okada also failed to teach about simultaneously performing lookup in both ITLB and DTLB. That is, Okada at best only appears to translate in parallel. It does not appear to perform the lookup in parallel.

(b) Mallick in view of Okada fails to disclose a TLB configured to operate in a processor having an Xscale core architecture. Mallick mentions specific architectures; however none of them is an Xscale core architecture. Okada doesn't mention any architecture at all.

Examiner respectfully traverses Applicant's remark for the following reasons:

In response to (a), Examiner disagree with Applicant. Even though Okada does not specifically recite about performing "lookup" in parallel, as admitted by Applicant and clearly recited in Okada, Okada does teach about translating both ITLB and DTLB in parallel. Examiner would like to point out to Applicant that the address/tag lookup is a part of the address translation process.

In response to (b), Examiner would like to point out to Applicant that Examiner interpreting the term "Xscale core architecture" as any type of architecture. Mallick discloses about operating TLB in a processor having Intel x86 architecture (see Col. 13, lines 13+).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Hsu et al. (6,430,675) discloses about performing parallel lookup of ITLB 106 and IP-to-TM cache 107 (see Col. 4, lines 40+ and Fig. 1).
- Chen et al. (USPN: 2009/0089768) teaches a DTLB and a ITLB configured to operate in a processor having an Xscale core architecture (see paragraph [0013]).

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HETUL PATEL whose telephone number is (571)272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hetul Patel/
Primary Examiner, Art Unit 2186